SUE Design Environment

Manage Your Design

- **Provides the framework for all design capture, simulation, timing, and data management**
- **Manages circuits, Verilog, documentation, and version control**
- **Drive third-party simulation tools**
- **Everything needed to manage current SoC design flow**

SUE design manager is a graphical environment that allows users to enter, visualize, and control large, complex chip designs. It is the first tool to combine HDL-based functional designs with structural design. This tool understands everything from Verilog to the operation and physical placement of transistors and wires.

Manage Your Design

The SUE design manager is not just another schematic capture tool. It is a complete design environment for capturing all levels and types of design information. It is a quantum leap in technology that gives the designer the ability to enter, visualize, and control large, complex chip designs.

Enter—Enter designs using the simple graphical user interface. RTL Verilog, gate-level, standard cell, or transistor-level descriptions can all be entered into the same schematic. The SUE design manager can be used from architectural analysis down to transistor-level schematics.

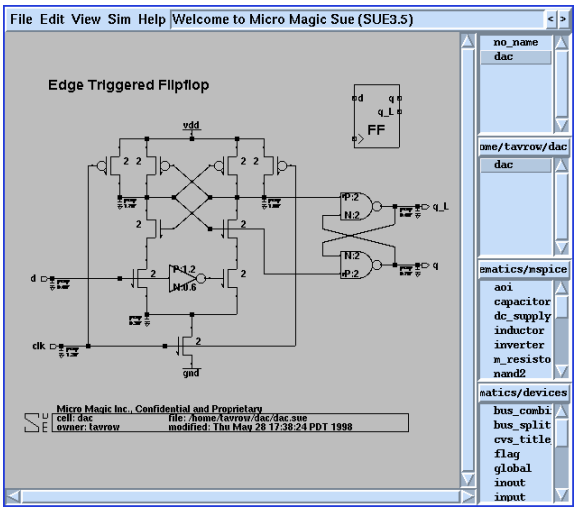
Visualize—The designer can quickly and easily browse all levels of the design hierarchy, pushing from the top level RTL description all the way down to the transistor-level with a click of the mouse. All Verilog, documentation, standard cell, and transistor level views can be observed from the same window.

Control—The SUE design manager is tightly integrated with other point tools and can launch them and review the results of their runs. It works interactively with most standard simulation and static timing analysis tools including Verilog, ADM, HSPICE, Pearl, PrimeTime, PathMill, and IRSIM. Simulation results are displayed right on the schematic. The interface is so seamless that in most cases a designer does not even need to learn how to run the other tool. From a single schematic, the SUE design manager can automatically generate SPICE, IRSIM, and Verilog netlists. It can also attach the behavioral model to the schematic. When doing higher-level Verilog simulations, the tools accept either the behavioral model or the schematic as input.

The capabilities of the SUE design manager can easily be extended and customized to fit into any design environment.

Power for All Types of Design

The SUE design manager is for the architect who needs quick prototyping. Quick visibility through all layers of logic and circuit design give the architect feedback to create high-performance architectures.



View the results of your simulation either directly on the schematic or in its waveform viewer.

This tool is for ASIC or semi-custom designers who cannot currently achieve their IC performance goals in acceptable time to market.

It is also useful for full-custom design organizations that want complete control and visibility at all levels of design and where performance is the name of the game. The SUE design manager was conceived and written by IC designers who wanted a better environment to do their jobs. Everything the designer needs to enter designs, netlist them, and interact with analysis tools is included as standard equipment.

SUE Features:

- Draw, view, and edit schematics, icons, graphics, and text.
- Automatically attach Verilog models and documentation to schematics.
- Automatically generate Verilog from schematic symbols and vice versa.
- Maintain multiple views (behavioral, RTL, structural) of schematics.
- Per-block choice of abstraction level at netlist time.
- Interactive cross-probing during simulation on schematic or waveform tool.
- Includes waveform viewer and reads/writes OVI-compliant Verilog files.
- ASCII database for transportability and ease of use with other programs and revision control.
- Standard netlist and simulator interfaces.
- Complete Tcl/Tk programming interface and API.
- Complete online documentation.
- EDIF interface (optional).
- Available on Linux and Solaris platforms.

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