MAX Layout Editor

The Intelligent Layout Environment

- **50 times faster.**
- **Production-proven database handles any size design.**
- **Real-time interactive DRC and connectivity tracing.**
- **Cross-probing between layout and schematic.**

MAX Layout Editor is an extremely fast, industrial strength, full-custom layout editor with the added benefit of a complete Tcl/Tk interface and API. MAX comes with continuous DRC, connectivity tracing, schematic cross-probing, wiring tool, extraction, schematic-driven layout, and more.

What Is MAX?

The MAX layout editor is much more than a layout tool. It is an intelligent IC layout environment. The MAX layout editor includes interactive cross-probing between layout and schematic. Automatic generation of layout from schematics, a feature of MAX-LS, provides true schematic-driven layout. With real-time interactive DRC, the MAX layout editor shows any DRC errors right on the layout. No memorizing of design rules or counting grids is required.

All this means that layout design is now easy and very fast, and cells are DRC clean. Automatic connectivity tracing from any layout source easily shows how elements are connected. No extraction is required.

In recent benchmarks, the MAX layout editor has proven to be 50 times faster in loading, displaying and editing physical layout data. It can handle the largest IC design databases with up to billions of devices.

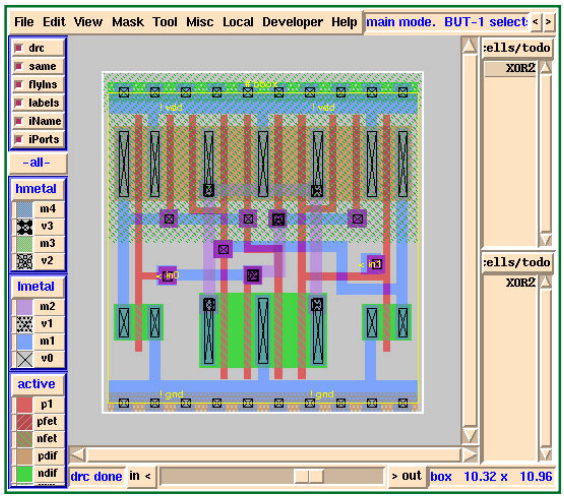
This tool is ideal for viewing and editing the results of place and route tools. When loading an entire chip before tapeout, the MAX layout editor accelerates the previously slow and torturous process of reviewing the entire design, the results of LVS and DRC checks, and any last-minute changes.

The MAX layout editor is adept at all aspects of physical design, from creating cells for a library, to interacting with place-and-route activities at the block-level, to assembling an entire chip. This tool has the power to handle the largest of chips, and it is easy to use. Designers will enjoy the view into the physical world that it offers.

View and Edit Full Chips Down to Full-custom Cells

The MAX layout editor is for physical design teams who need to view, manipulate, and understand what is going on with their place-and-route process.

It is also useful for integration teams who need to efficiently manipulate large amounts of data during assembly and perform back-end analyses.



MAX Layout Environment — View and edit the largest designs.

This tool has a number of features that make it the best choice for doing IC layout for high-performance, fast time-to-market designs. best choice for doing IC layout for high-performance, fast time-to-market designs.

MAX Features:

- Fastest Schematic Driven Layout System for any size IC.
- Continuous DRC, real-time feedback means mask designers don't need to waste time learning new design rules.
- Interactive connectivity always available.
- Interactive wiring tool with flylines to show connections.
- Generators for layout ranging from simple transistors and gates to large structures (e.g. SRAMs.)
- Hierarchical and incremental parasitic extraction.
- Reads/Writes LEF/DEF, and GDSII formats.
- Interfaces to industry standard DRC and LVS tools.
- Full customization and extensions via Tcl/Tk and a full API. - Usable out of the box, or customize as you wish. - Write interfaces to all the other tools in your design flow.
- Optimized for large databases.
- ASCII database for transportability and ease of use with other programs, scripts, and user's choice of revision control systems.
- SRAM Compiler Tool extension. Many other features too numerous to list.
- Available on Linux and Solaris platforms.

Micro Magic Inc.

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