DPC Datapath Compiler

The Tool for High Performance Designs

- **ASIC performance of a custom design**
- **Data paths are three times faster than custom ASIC design**
- **Data paths are 40% smaller than custom ASIC design**
- **One-tenth the effort of full-custom design**

The DataPath compiler generates data paths from a schematic view and back-annotate accurate timing information onto the schematic in seconds. It can place custom-style “bit-slice” data paths, minimizing wire lengths for high performance, and can even include control logic, all using an existing standard cell library.

The Tool for High-Performance Designs

The DataPath compiler is the tool of choice for designers of high-performance chips. It provides the performance of full-custom design, but with a much shorter design cycle. Data paths designed with the DataPath compiler are three times faster and 40% smaller than synthesis and place and route, and they take one-tenth the effort of full-custom design.

In deep sub micron design, wire length is the dominant factor affecting critical-path timing, and cell placement plays a major role in chip performance. With traditional tools, designers are at the mercy of automatic placement tools. The DataPath compiler provides fine control over placement, giving immediate timing feedback and allowing multiple what-if experiments to be performed. The DataPath compiler graphical display which back-annotates timing to the schematic, allows easy identification of timing problems and rapid iteration through potential solutions. The DataPath compiler is so fast that it can place and then time a 50,000-gate data path in about two minutes.

Useful Identification of Critical Paths

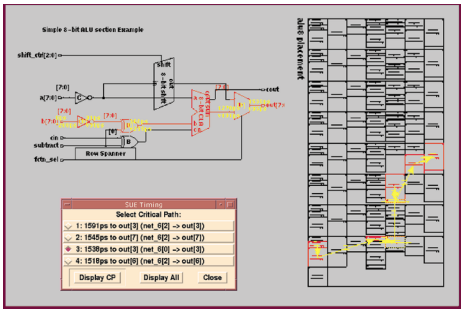
The DataPath compiler predicts wire lengths early in the design cycle. The resulting timing iterations are both fast and accurate, allowing designers to quickly iterate to their performance goal. The critical paths are displayed directly on the schematic at all levels of the design hierarchy. In addition, the actual delays of the paths are annotated onto the wires in both the schematic and placement views.

Optimization of Critical Paths

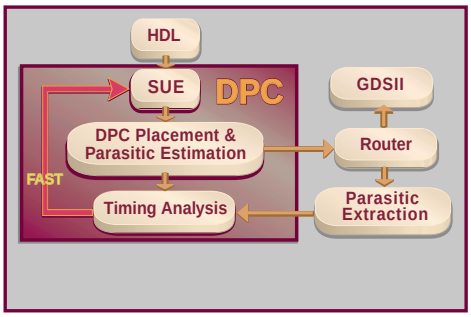
The DataPath compiler allows designers to easily specify and modify simple directives to produce speed-optimized layouts when doing data path design. These directives are easily given and modified in the compiler. The placement of components on the schematic directs relative placement in the placement file.

Designers can place cells at specific row or column locations and can indicate empty space. The DataPath compiler automatically generates the row and column placement and the predicted wire lengths. Wire predictions can be used to drive timing analyzers including Pearl, PrimeTime, and PathMill.

The DataPath compiler reads the output from static timing analysis and displays the critical paths directly on the schematic. Designers can modify the placement to optimize critical paths or can add extra drivers to the critical path, all in the schematic. Designers can then



This example shows the placement generated for our sample 8-bit ALU. A critical path is highlighted in red and yellow. Timing for other nets is indicated in the menu. New nets can be selected and highlighted.



The DataPath compiler reduces (from days to minutes) the time required for placement and timing analysis.

iterate through the placement and timing until the timing criteria are satisfied. The iteration loop is fast and visual. When the design performance is satisfactory, the placement (DEF) file is passed to a routing tool. The routed result can then be read into the MAX layout editor to view and edit if necessary.

Design Flow

With the DataPath compiler, design begins with entering schematics into the SUE design manager. The compiler then uses the schematic as a basis for placement. When the placement is complete, the DataPath compiler estimates the wiring delays and sends this information to a static timing analyzer. The SUE design manager reads the results of the static timing analysis. The critical path is highlighted in both the schematic and the placement view, and the delay and slope at each node are displayed.

DPC Features

- Automatically generates parasitics, runs timing verifiers, and displays critical-path timing directly on schematics.
- Integrated with static timing analysis tools including Pearl, PathMill, and PrimeTime.
- Operates quickly, placing and timing a 50,000-gate data path in just a few minutes.
- Uses standard cells or custom data path cells.
- Writes DEF placement information and Verilog netlists for integration with routing tools.
- Available on Linux and Solaris platforms.

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