MAX-LS Layout System The Tool for Layout Designers

- 50 times faster.
- Production-proven database handles any size design.
- Real-time interactive DRC and connectivity tracing.
- Cross-probing between layout and schematic.

The MAX-LS layout system is a Micro Magic tool that incorporates our best tools for IC physical layout design of leaf cells, large blocks, and complete SoC products, and adds schematic-driven layout.

This tool has all the capabilities of the standard MAX layout editor, plus it has a schematic viewer and layout generator.

What Is MAX-LS?

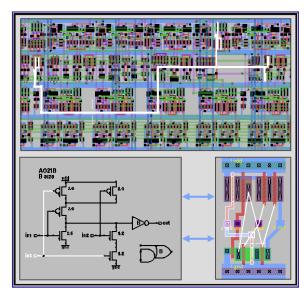
The MAX-LS layout system is ideal for full custom IC layout designers who are working on the largest, fastest, state-of-the-art digital or analog IC designs. It provides a complete environment to receive information from design engineering and to contain all technology information from a specific foundry. The physical layout process goes faster when using the MAX-LS layout system.

This tool provides all the capabilities necessary for layout designers to accomplish their mission.

It features true schematic-driven layout design, offering the ability to interactively generate a layout that is DRC- and LVS-correct with devices automatically sized.

Based on a schematic, the MAX-LS layout system can generate every transistor, show flylines for connecting them, and cross-probe between schematic and layout. This gives the layout designer complete control, yet assures rapid physical design development.

Both the MAX layout editor and the MAX-LS layout system tools have complete programming interfaces using Tcl/Tk and a well-documented API. Whether you need full-custom layout, cell-assembly, chip-assembly, or the ability to write your own generators, these are the tools to choose for your physical design needs.



Schematic-driven layout generation, cross-probing between layout and schematic, interactive connectivity tracing and real-time DRC.

MAX-LS Features:

- Fastest Schematic Driven Layout System for any size IC.
- Only IC Layout Product that combines real-time DRC, interactive cell layout generation, and cross-probing between schematic and layout.
- Offers superior ease of learning and use.
- All-angle capability.
- · Interactive wiring tool.
- Interactive connectivity tracing.
- · Continuous, real-time DRC checking.
- Complete TcI/Tk interface and a complete API.
- Easy integration with other tools. GDSII, LEF/DEF.
- Complete on-line documentation and tutorial.
- Available on Linux and Solaris platforms.